

SUPER MUSIC CARD

"MUSTALGAME"

## INSTALLATION

Just plug your MUSTALGAME card into the slot specified by the software ( usually slot 4 ). Connect the jet of the stereo speaker provided and then RUN your software. Adjust the individual Volume of each channel for loudness.

If you want to amplify the sound further using your own power amplifier, connect the inputs of the amplifier to the LINE-OUTs of the MUSTALGAME. You can get the best sound effects.

To play save turn your computer's power supply off while you are doing insertions or connections.

## PROGRAMMING

The MUSTALGAME can be programmed to produce various types of sound including musical note, game sound effects and human voice.

The hardware that actually produces the sound is GI's sound generation chip AY-3-891X. Therefore it is very important to know how to programme the sound chip.

There are 16 registers within the sound chip which is listed below:-

<u>Register</u>	<u>Description</u>
R0	Channel A Freq Fine tune ( 8 bits )
R1	Channel A Freq Coarse tune ( 4 bits )
R2	Channel B Freq Fine tune ( 8 bits )
R3	Channel B Freq Coarse tune ( 4 bits )
R4	Channel C Freq Fine tune ( 8 bits )
R5	Channel C Freq Coarse tune ( 4 bits )
R6	Noise Freq ( 5 bits )
R7	Enable ( 8 bits )
R8	Channel A Amplitude ( 5 bits )
R9	Channel B Amplitude ( 5 bits )
R10	Channel C Amplitude ( 5 bits )
R11	Envelope Period Fine tune ( 8 bits )
R12	Envelope Period Coarse tune ( 8 bits )
R13	Envelope Shape / Cycle ( 4 bits )
R14	I / O Port X ( 8 bits )
R15	I / O Port Y ( 8 bits )

APPLE ADDRESS

FUNCTION

\$C400 Speaker 1 Function Select  
 \$C480 Speaker 2 Function Select  
  
 \$C401 Speaker 1 Data In/Out  
 \$C481 Speaker 2 Data In/Out

-----  
 \$C400 : : X : X : X : X : X : B2 : B1 : B0 :  
 -----

0	X	X		Reset
1	1	1		
1	0	0		Select Register
1	1	0		
1	0	0		Latch Data

-----  
 \$C401 : : X : X : X : X : B3 : B2 : B1 : B0 :  
 -----

Select Register :	0	0	0	0	R0
	To				
	1	1	1	1	R15

-----  
 \$C401 : : B7 : B6 : B5 : B4 : B3 : B2 : B1 : B0 :  
 -----

Latch Data :	0	0	0	0	0	0	0	0	Value 0
	To								
	1	1	1	1	1	1	1	1	Value 255

Register

Description

R0,R1 : CH.A Freq 1 ( 63.94KHz ) to 4095 ( 15.6Hz )  
 R2,R3 : CH.B Freq 1 ( 63.94KHz ) to 4095 ( 15.6Hz )  
 R4,R5 : CH.C Freq 1 ( 63.94KHz ) to 4095 ( 15.6Hz )  
 R6 : Noise Freq 1 ( 63.94KHz ) to 31 ( 2.06KHz )  
 R7 : ENABLE BIT 0 : 0 = TONE A ENABLE ( SPEAKER 1 )  
 BIT 1 : 0 = TONE 1 ( 63.94KHz ) to 4095 ( 15.6Hz )  
 R4,R5 : CH.C Freq 1 ( 63.94KHz ) to 4095 ( 15.6Hz )  
 R6 : Noise Freq 1 ( 63.94KHz ) to 31 ( 2.06KHz )  
 R7 : ENABLE BIT 0 : 0 = TONE A ENABLE ( SPEAKER 1 )  
 BIT 1 : 0 = TONE B ENABLE ( SPEAKER 1 )  
 BIT 2 : 0 = TONE C ENABLE ( SPEAKER 1 )  
 BIT 3 : 0 = NOISE A ENABLE ( SPEAKER 1 )  
 BIT 4 : 0 = NOISE B ENABLE ( SPEAKER 1 )  
 BIT 5 : 0 = NOISE C ENABLE ( SPEAKER 1 )  
 BIT 6 : 0 = OUTPUT TO PORT X ( SPEAKER 1 )  
 BIT 7 : 0 = OUTPUT TO PORT Y ( SPEAKER 2 )  
 R8 : CH.A Amplitude level = 0 to 15 ; > 16 amplitude define by R13  
 R9 : CH.B Amplitude level = 0 to 15 ; > 16 amplitude define by R13  
 R10 : CH.C Amplitude level = 0 to 15 ; > 16 amplitude define by R13  
 R11,R12 : Envelope Freq 1 ( 3996Hz ) to 65535 ( 0.061Hz )  
 R13 : Envelope Shape / Cycle : BIT 0 : HOLD  
 BIT 1 : ALTERNATE  
 BIT 2 : ATTACK  
 BIT 3 : CONTINUE  
 R14 : PORT X DATA REGISTER : FOR 8 BIT D/A CONVERT  
 R15 : PORT Y DATA REGISTER : FOR 8 BIT D/A CONVERT

## THE DEFINITION OF EACH FUNCTION

**HOLD** When set to logic "1", limits the envelope to one cycle, holding the last count of the envelope counter ( E3--E0==0000 or 1111, depending on whether the envelope counter was in a count-down or count-up mode, respectively ).

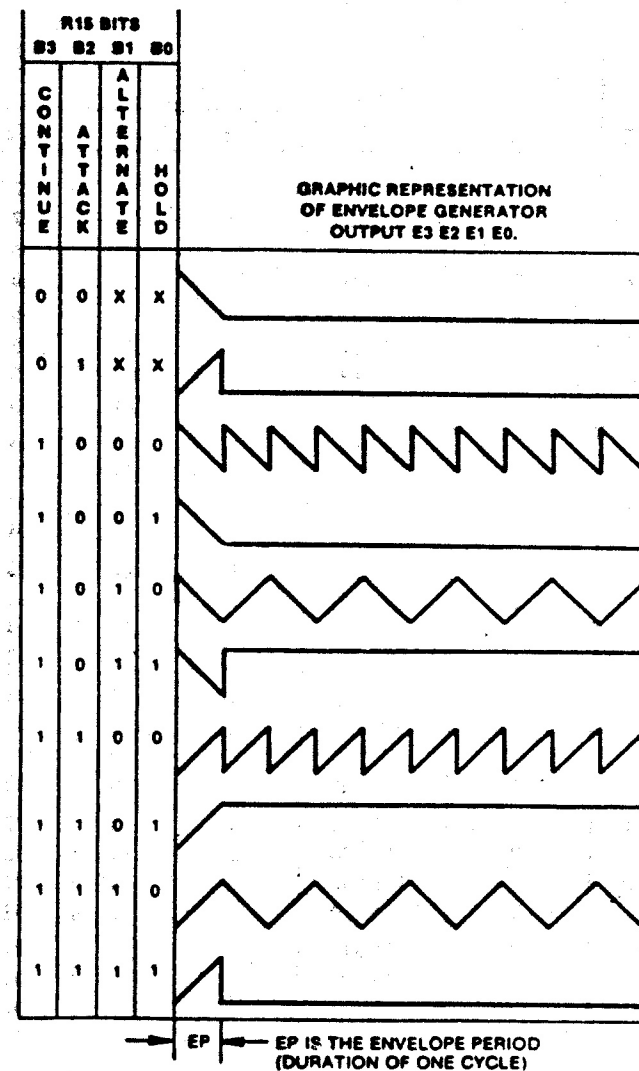
**ALTERNATE** When set to logic "1", the envelope counter reverses count direction ( up-down ) after each cycle.

**ATTACK** When set to logic "1", the envelope counter will count up ( attack ) from E3 E2 E1 E0 == 0000 to E3 E2 E1 E0 == 1111; when set to logic "0", the envelope counter will count down ( decay ) from 1111 to 0000.

**CONTINUE** When set to logic "1", the cycle pattern will be as defined by the Hold bit; when set to logic "0", the envelope generator will reset to 0000 after one cycle and hold at that count.

**NOTE :** When both the Hold bit and the Alternate bit are ones, the envelope counter is reset to its initial count before holding.

## ENVELOPE SHAPE/CYCLE CONTROL



**APPENDIX** Equal Tempered Chromatic Scale  
(ICLOCK- 1,023 MHz)  
(adapted from General Instrument Programmable Sound Generator Data Manual)

NOTE	OCTV	NOTE FREQ	TONE PERIOD			
			(DEC)		(HEX)	
			CRSE	FINE	CRSE	FINE
C	1	32.703	7	163	07	A3
C#	1	34.648	7	53	07	35
D	1	36.708	6	205	06	CD
D#	1	38.891	6	108	06	6C
E	1	41.203	6	15	06	0F
F	1	43.654	5	184	05	88
F#	1	46.249	5	102	05	66
G	1	48.999	5	24	05	18
G#	1	51.913	4	207	04	CF
A	1	55.000	4	138	04	BA
A#	1	58.270	4	73	04	49
B	1	61.735	4	11	04	08
C	2	65.406	3	209	03	D1
C#	2	69.296	3	154	03	9A
D	2	73.416	3	102	03	66
D#	2	77.782	3	54	03	36
E	2	82.406	3	7	03	07
F	2	87.308	2	220	02	DC
F#	2	92.498	2	179	02	B3
G	2	97.998	2	140	02	8C
G#	2	103.826	2	103	02	67
A	2	110.000	2	69	02	45
A#	2	116.540	2	36	02	24
B	2	123.470	2	5	02	05
C	3	130.812	1	232	01	E8
C#	3	138.592	1	205	01	CD
D	3	146.832	1	179	01	B3
D#	3	155.564	1	155	01	9B
E	3	164.812	1	131	01	83
F	3	174.616	1	110	01	6E
F#	3	184.996	1	89	01	59
G	3	195.996	1	70	01	46

**APPENDIX** Equal Tempered Chromatic Scale (continued)  
(ICLOCK- 1,023 MHz)

NOTE	OCTV	NOTE FREQ	TONE PERIOD			
			(DEC)		(HEX)	
			CRSE	FINE	CRSE	FINE
G#	3	207.652	1	51	01	33
A	3	220.000	1	34	01	22
A#	3	233.080	1	18	01	12
B	3	246.940	1	2	01	02
C	4	261.624	0	244	00	F4
C#	4	277.184	0	230	00	E6
D	4	293.664	0	217	00	D9
D#	4	311.128	0	205	00	CD
E	4	329.624	0	193	00	C1
F	4	349.232	0	183	00	B7
F#	4	369.992	0	172	00	AC
G	4	391.992	0	163	00	A3
G#	4	415.304	0	153	00	99
A	4	440.000	0	145	00	91
A#	4	466.160	0	137	00	89
B	4	493.880	0	129	00	81
C	5	523.248	0	122	00	7A
C#	5	554.368	0	115	00	73
D	5	587.328	0	108	00	6C
D#	5	622.256	0	102	00	66
E	5	659.248	0	96	00	60
F	5	698.464	0	91	00	5B
F#	5	739.984	0	86	00	56
G	5	783.984	0	81	00	51
G#	5	830.608	0	76	00	4C
A	5	880.000	0	72	00	48
A#	5	932.320	0	68	00	44
B	5	987.760	0	64	00	40
C	6	1046.496	0	61	00	3D
C#	6	1108.736	0	57	00	39
D	6	1174.656	0	54	00	36
D#	6	1244.512	0	51	00	33

APPENDIX Equal Tempered Chromatic Scale (continued)  
(FCLOCK- 1.023 MHz)

NOTE	OCTV	NOTE FREQ	TONE PERIOD			
			(DEC)		(HEX)	
			CRSE	FINE	CRSE	FINE
E	6	1318.496	0	48	00	30
F	6	1396.928	0	45	00	2D
F#	6	1479.968	0	43	00	2B
G	6	1567.968	0	40	00	28
G#	6	1661.216	0	38	00	26
A	6	1760.000	0	36	00	24
A#	6	1864.640	0	34	00	22
B	6	1975.520	0	32	00	20
C	7	2092.992	0	30	00	1E
C#	7	2217.472	0	28	00	1C
D	7	2349.312	0	27	00	1B
D#	7	2489.024	0	25	00	19
E	7	2636.992	0	24	00	18
F	7	2793.856	0	22	00	16
F#	7	2959.936	0	21	00	15
G	7	3135.936	0	20	00	14
G#	7	3322.432	0	19	00	13
A	7	3520.000	0	18	00	12
A#	7	3729.280	0	17	00	11
B	7	3951.040	0	16	00	10
C	8	4185.984	0	15	00	0F
C#	8	4434.944	0	14	00	0E
D	8	4698.624	0	13	00	0D
D#	8	4978.048	0	12	00	0C
E	8	5273.984	0	12	00	0C
F	8	5587.712	0	11	00	0B
F#	8	5919.872	0	10	00	0A
G	8	6271.872	0	10	00	0A
G#	8	6644.864	0	9	00	09
A	8	7040.000	0	9	00	09
A#	8	7458.560	0	8	00	08
B	8	7902.080	0	8	00	08

APPENDIX Assembly Language Program Listings

1	*PRIMARY ROUTINES		
2	*FOR SLOT 4		
3	*		
4		ORG \$9000	
5	*		ADDRESSES FOR FIRST
6	ORB	EQU \$C400	:PORT B
7	ORA	EQU \$C401	:PORT A
8	DDRB	EQU \$C402	:DATA DIRECTION REGSTR (B)
9	DDRA	EQU \$C403	:DATA DIRECTION REGSTR (A)
10	*		ADDRESSES FOR SECOND
11	ORB2	EQU \$C480	:PORT B
12	ORA2	EQU \$C481	:PORT A
13	DDRB2	EQU \$C482	:DATA DIRECTION REGSTR (B)
14	DDRA2	EQU \$C483	:DATA DIRECTION REGSTR (A)
15	*		
16	*ROUTINES FOR FIRST		
17	*		
18	INIT	LDA #\$FF	:SET PORT A FOR OUTPUT
9000:	A9 FF		
9002:	BD 03 C4 19	STA DDRA	
9005:	A9 07 20	LDA #\$07	:SET PORT B FOR OUTPUT
9007:	BD 02 C4 21	STA DDRB	
900A:	60 22	RTS	:RETURN
23	*		

APPENDIX Assembly Language Program Listings (continued)

```

900B: A9 07 24 LATCH LDA #S07 ;SEND "LATCH
          ;COMMAND"
900D: 8D 00 C4 25 STA ORB ;TO SOUND
9010: A9 04 26 LDA #S04 ;THROUGH
          ;PORT B
9012: 8D 00 C4 27 STA ORB
9015: 60 28 RTS ;RETURN
          29 *
9016: A9 06 30 WRITE LDA #S06 ;SEND "WRITE
          ;COMMAND"
9018: 8D 00 C4 31 STA ORB ;TO SOUND
901B: A9 04 32 LDA #S04 ;THROUGH
          ;PORT B
901D: 8D 00 C4 33 STA ORB
9020: 60 34 RTS ;RETURN
          35 *
9021: A9 00 36 RESET LDA #S00 ;SEND "RESET
          ;COMMAND"
9023: 8D 00 C4 37 STA ORB ;TO SOUND
9026: A9 04 38 LDA #S04 ;THROUGH
          ;PORT B
9028: 8D 00 C4 39 STA ORB
902B: 60 40 RTS ;RETURN
          41 *
          42 *ROUTINES FOR SECOND
          43 *
902C: A9 FF 44 INIT2 LDA #SFF ;SET PORT A
          ;FOR OUTPUT
902E: 8D 83 C4 45 STA DDRA2
9031: A9 07 46 LDA #S07 ;SET PORT B
          ;FOR OUTPUT
9033: 8D 82 C4 47 STA DDRB2
9036: 60 48 RTS ;RETURN
          49 *

```

APPENDIX Assembly Language Program Listings (continued)

```

9037: A9 07 50 LATCH2 LDA #S07 ;SEND "LATCH
          ;COMMAND"
9039: 8D 80 C4 51 STA ORB2 ;TO SOUND
903C: A9 04 52 LDA #S04 ;THROUGH
          ;PORT B
903E: 8D 80 C4 53 STA ORB2
9041: 60 54 RTS ;RETURN
          55 *
9042: A9 06 56 WRITE2 LDA #S06 ;SEND "WRITE
          ;COMMAND"
9044: 8D 80 C4 57 STA ORB2 ;TO SOUND
9047: A9 04 58 LDA #S04 ;THROUGH
          ;PORT B
9049: 8D 80 C4 59 STA ORB2
904C: 60 60 RTS ;RETURN
          61 *
904D: A9 00 62 RESET2 LDA #S00 ;SEND "RESET
          ;COMMAND"
904F: 8D 80 C4 63 STA ORB2 ;TO SOUND
9052: A9 04 64 LDA #S04 ;THROUGH
          ;PORT B
9054: 8D 80 C4 65 STA ORB2
9057: 60 66 RTS ;RETURN

```

1 \*TABLE ACCESS ROUTINE  
2 \*FOR SLOT 4  
3 \*  
4 ORG \$8000  
5 \*  
6 PTR EQU \$08 ;DATA  
7 ORA EQU \$C401 ;PORT A  
8 LATCH EQU \$900B ;LATCH SUB-  
ROUTINE

APPENDIX Assembly Language Program Listings (continued)

```

9 WRITE EQU $9016 ;WRITE SUB-
;ROUTINE
10 RESET EQU $9021 ;RESET SUB-
;ROUTINE
11 * ;ADDRESSES
;FOR SECOND

12 PTR2 EQU $0A ;DATA
;PTRER
13 ORA2 EQU $C481 ;PORT A
14 LATCH2 EQU $9037 ;LATCH SUB-
;ROUTINE
15 WRITE2 EQU $9042 ;WRITE SUB-
;ROUTINE
16 RESET2 EQU $904D ;RESET SUB-
;ROUTINE

17 *
18 *ROUTINES FOR FIRST
19 *
8000: 20 21 90 20 START JSR RESET ;RESET SOUND
8003: A0 00 21 LDY #$00 ;USED TO IDEN-
;TIFY REGIS-
;TER
8005: 8C 01 C4 22 LOOP STY ORA ;# OF SOUND

8008: 20 08 90 23 JSR LATCH
8008: B1 08 24 LDA (PTR),Y ;GET DATA
;FROM TABLE

800D: 8D 01 C4 25 STA ORA
8010: 20 16 90 26 JSR WRITE ;STORE IN REG-
;ISTER

8013: C0 0F 27 CPY #$0F ;END OF DATA?
8015: F0 04 28 BEQ DONE ;YES, EXIT
8017: C8 29 INY
8018: 4C 05 80 30 JMP LOOP ;NO. GET NEXT
;SET

```

APPENDIX Assembly Language Program Listings (continued)

```

801B: 60 31 DONE RTS ;RETURN
;
;32 *
;33 *ROUTINES FOR SECOND
;34 *
801C: 20 4D 90 35 START2 JSR RESET2 ;SAME
;INSTRUC-
;TIONS AS
;ABOVE

801F: A0 00 36 LDY #$00
8021: 8C 81 C4 37 LOOP2 STY ORA2
8024: 20 37 90 38 JSR LATCH2
8027: B1 0A 39 LDA (PTR2),Y
8029: 8D 81 C4 40 STA ORA2
802C: 20 42 90 41 JSR WRITE2
802F: C0 0F 42 CPY #$0F
8031: F0 04 43 BEQ DONE2
8033: C8 44 INY
8034: 4C 22 80 45 JMP LOOP2
8037: 60 46 DONE2 RTS

1 ;*PROCESSOR LOOP
2 ;*FOR LASER AND BOMB
3 ;*SOUND EFFECT
4 ;
5 ; ORG $8F00
6 ;
7 ; ;FOR SECOND

8 PTR EQU $08 ;DATA POINTE
9 TONE EQU $0A ;TONAL VALUE
10 TIME EQU $0B ;TIME VALUE
;FOR DELAY

11 BASE EQU $C400 ;CARD
;ADDRESS

12 ORA EQU BASE + 1 ;PORT A
13 TAR EQU $8000 ;TABLE ACCESS
;ROUTINE
14 LATCH EQU $900B ;LATCH SUB-
;ROUTINE

```



APPENDIX Assembly Language Program Listings (continued)

	15	WRITE	EQU	\$9016	:WRITE SUB-ROUTINE
	16	RESET	EQU	\$9021	:RESET SUB-ROUTINE
	17	WAIT	EQU	\$FCA8	:WAIT SUBROUTINE
	18	.			
	19	.			
8F00:	A9	00	LDA	#\$00	:LOAD HIGHEST
8F02:	85	0A	STA	TONE	:FREQUENCY
					VALUE
8F04:	A9	0F	LDA	#\$0F	:LOAD SHORT
8F06:	85	08	STA	TIME	:TIME DELAY
8F08:	4C	13	JMP	START	:AND START
8F0B:	A9	30	LDA	#\$30	:LOAD MIDDLE
8F0D:	85	0A	STA	TONE	:FREQUENCY
					VALUE
8F0F:	A9	40	LDA	#\$40	:LOAD LONGER
8F11:	85	08	STA	TIME	:TIME DELAY
8F13:	A9	90	LDA	#\$90	:SET TABLE
					ADDRESS
8F15:	85	08	STA	PTR	
8F17:	A9	81	LDA	#\$81	
8F19:	85	09	STA	PTR + 1	
8F1B:	20	00	JSR	TAR	:TRANSFER
					DATA
8F1E:	A9	00	LDA	#\$00	:LATCH FIRST
					REGISTER
8F20:	8D	01	STA	ORA	:ADDRESS
8F23:	20	0B	JSR	LATCH	
8F26:	A5	0A	LDA	TONE	:GET TONE
					VALUE
8F28:	8D	01	STA	ORA	:STORE IN REG-
					ISTER
8F2B:	20	16	JSR	WRITE	
8F2E:	A5	0B	LDA	TIME	:GET TIME
					VALUE

APPENDIX Assembly Language Program Listings (continued)

8F30:	20	A8	FC	41	JSR	WAIT	:AND DELAY
8F33:	E6	0A		42	INC	TONE	:INCREMENT
							TONE VALUE
8F35:	A9	FF		43	LDA	#\$FF	:END OF
							INCREASE?
8F37:	C5	0A		44	CMP	TONE	
8F39:	F0	03		45	BEQ	DONE	:YES, EXIT
8F3B:	4C	26	8F	46	JMP	LOOP	:NO, START
							AGAIN
8F3E:	A5	0B		47	DONE	LDA	TIME
							:GET TIME
							VALUE
8F40:	20	A8	FC	48	JSR	WAIT	:DELAY
8F43:	A9	00		49	LDA	#\$00	:RESTORE
							ORIGINAL
8F45:	85	0A		50	STA	TONE	:TONE VALUE
8F47:	20	21	90	51	JSR	RESET	:CLEAR SOUND
							CHIP
8F4A:	60			52	RTS		:REGISTERS
							AND
							RETURN

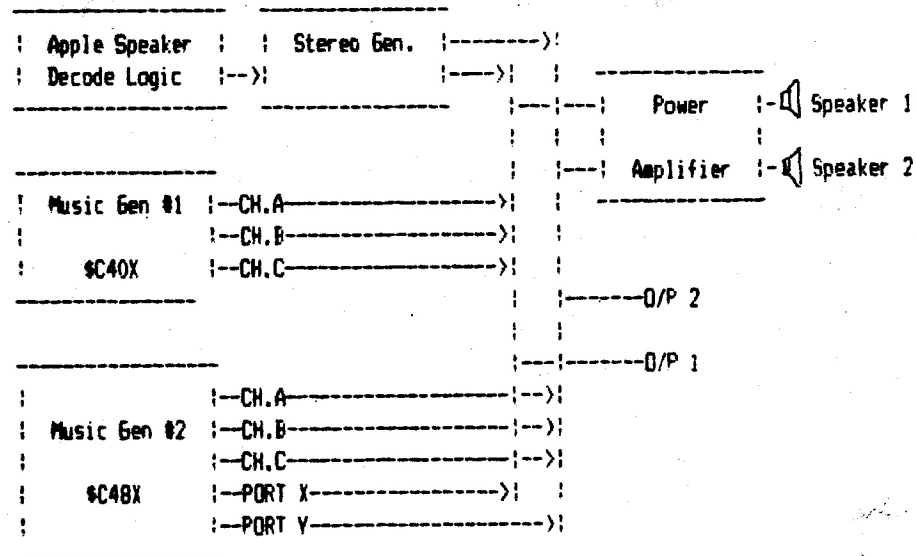
## THE MUSTALGAME CARD

The name stands for MUSIC, TALK and GAME SOUND EFFECTS. It generates a remarkable array of sound effects and music. It is a programmable sound generations system that enhances your APPLE II computer's sound capability. Moreover it can also be used as a dual channel talk card to produce human voice.

Hundreds of software were written especially for this MUSTALGAME card. It includes:-

- . MUSIC CONSTRUCTION SET
- . MUSIC SYNTHESIZER
- . MOCKING BOARD DEMONSTRATION SOFTWARE
- . LOTS OF GAMES LIKE POPPYE, LADY TUDE, SPYSTRIKES, TONY WAR.....ECT.
- . R.A.M. Remote Automatic Mouth, Cantonese, Speak and Spell

What's more, it also amplifies the APPLE II's own speaker voice and change it into stereophonic sound . Therefore all the game that produce sound is suitable but there is no need for any interconnecting cable.



BLOCK DIAGRAM OF MUSTALGAME